Project Plan
High-Resolution ADC Using Delta-Sigma Architectures
Version 3

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Table of Contents

1 Frontal Material

1.1 List of Figures

1.2 List of Definitions

Integrated circuit (IC) – an electronic circuit formed on a piece of semiconducting material.[1]

Analog to digital converter (ADC) – an electronic device that converts an analog signal to a digital signal without altering its essential content.[2]

Throttle – control the operation speed of a circuit, and therefore its heat dissipation rate.

Sample – reduce a continuous-time signal to a discrete-time signal by collecting a series of its values at regularly spaced intervals.[3]

Resolution – the number of discrete output values an ADC can produce over the range of analog input values.[4]

Delta-sigma ADC – an ADC that produces a high-resolution output signal using oversampling techniques.[5]

DAC – an electronic device that converts a digital signal to an analog signal without altering its essential content.[6]

Modulator – an electronic device that varies one or more properties of a periodic waveform.[7]

Digital Decimator – a device that reduces the sampling rate of a digital signal.[8]

Parasitic Capacitance – a usually unwanted capacitance that exists between parts of electronic components or circuits because of their proximity to each other.[9]

Switched Capacitor Integrator – an electronic device that performs an integrating function using an operational amplifier and a switch-connected capacitor that acts as a current-limiting component.

Comparator – an electronic circuit that compares two voltages and outputs a digital signal indicating which voltage is larger.[10]

Layout – a representation of an integrated circuit using geometric shapes that correspond to the patterns of the materials that make up the physical integrated circuit.[11]

2 Introductory Material

2.1 Acknowledgement

The development of this design is supported by faculty advisor Dr. Randall Geiger. We would like to thank Dr. Geiger for providing the key insight and expertise that greatly assists our project. His contributions are crucial in ensuring that our team fully comprehends the necessary technical material for this project.

2.2 Problem Statement

We rely heavily on various integrated circuits (IC) to perform as intended every day. Without these circuits, we would have a difficult time with typical day to day tasks. Heat can become a serious issue with ICs. When these chips overheat, it can damage the circuit and cause it to malfunction. There is a need for a method to measure and communicate the chip temperature to circuitry that will throttle the circuit activity when necessary.

Our team has proposed to design a temperature sensor and a delta-sigma analog-to-digital converter (ADC) to convert the temperature sensor's output to a digital signal. This circuit will accurately measure, and communicate in a digital format, the temperature of the IC. With this technology, the temperature of an IC can be monitored and controlled as it is being used to ensure that it doesn't overheat.

2.3 Operating Environment

Our circuit can be integrated with any IC as it is intended to monitor the temperature of that IC. The operating environment will vary depending on the system the circuit is integrated with. For most purposes, this will result in the circuit being used in a small enclosed environment.

2.4 Intended Users and Intended Uses

Our product is to be used by IC designers when designing new ICs. They will integrate our circuit with the IC they are designing. The circuit is intended to be used by IC designers in both industry and in academic research.

Our product will be used to measure and communicate the temperature of an IC to other parts of the IC responsible for temperature control. Based on the output of our circuit, the connected circuitry will change the IC's rate of activity to reduce heat dissipation when the temperature rises above a certain threshold.

2.5 Assumptions and Limitations

Assumptions:

- The temperature of the IC in which the temperature sensor and ADC are used will remain between 10 degrees and 60 degrees Celsius.
- Two accurate reference voltages of 765 millivolts and 800 millivolts will be provided to the ADC.

Limitations:

- The area of the physical layout of the circuit is no more than 4 millimeters by 4 millimeters.
- The supply voltage is 0V to 1.8 V.

2.6 Expected End Product and Other Deliverables

The ADC will be a fabricated IC containing our ADC and temperature sensor. It will be fabricated through MOSIS over the summer of 2018. The fabrication will be completed by August 2018 to allow our team to test for functionality of the IC during the Fall 2018 semester.

We will also produce an assessment of the performance capabilities and limitations of over-sampled data converters, testing results for our complete circuit, and an assessment of the overall performance of the ADC and the temperature sensor based upon the experimental results and their relation to the simulation results.

3 Proposed Approach and Statement of Work

3.1 Proposed Approach

- **3.1.1 Functional Requirements:** The ADC should sample the input voltage signal at 102.4 kHz, and output 10-bit digital codes at a rate of one per 10 milliseconds. The output codes' magnitudes should be proportional to the input voltage relative to a 730 millivolt to 800 millivolt range.
- **3.1.2 Constraints Consideration:** During the first semester, the team will be on a time constraint to deliver the design to be fabricated by the first week of June. The circuit will be designed in the TSMC 0.18 µm process and have a resolution of 10 bits.
- **3.1.3 Technology Consideration:** Cadence Virtuoso will be the main design software and will be provided by the Electrical and Computer Engineering department at Iowa State University. Device fabrication will be done through MOSIS in a 0.18 µm process. The die size will be 4mm x 4mm.
- **3.1.4 Testing Requirements Consideration:** Upon fabrication, the IC will be tested to validate simulation results using existing laboratory equipment at Iowa State University. Tests to determine the spectral characteristics and quality of the data converter will also take place.
- **3.1.5 Safety Consideration:** This design project should not pose any safety concerns.
- **3.1.6 Previous Work:** There are a large variety of data converter architectures that are currently available. This project specifically asked for the design of a delta-sigma data converter although other designs considered were a SAR and Nyquist rate data converter. The SAR (Successive-approximation) data converter is one of the oldest and most common data converter architectures. The SAR is used when there are multiple inputs, and it is mainly implemented in industrial control applications. The Nyquist data

converters are data converters sampled at the Nyquist rate frequency. These data converters cannot reach a high resolution and experience a higher level of quantization noise at the output. The chosen design, the Delta Sigma ADC, has characteristics that make it the best fit for our application of measuring the voltage output of a temperature sensor. The delta-sigma ADC experiences a low level of quantization noise at the output. This is achieved through oversampling of the input signal. The Delta Sigma architecture produces a high-resolution output, which will provide an accurate temperature reading from our sensor. Our delta-sigma ADC design is based on the design in the textbook *Analog Integrated Circuit Design*[12]. We modified the design to use first-order modulator and decimator circuits instead of higher-order circuits. The first-order circuit is sufficient for providing the desired output and makes the circuit design much simpler. The tradeoff is that a first-order circuit will not carry out noise shaping in the ADC which would result in a more accurate output, which is exemplified in the *IEEE Journal of Solid-State Circuits* article, "A 43-mW MASH 2-2 CT ΣΔ Modulator Attaining 74.4/75.8/76.8 dB of SNDR/SNR/DR and 50 MHz of BW in 40-nm CMOS."[13]

- **3.1.7 Possible Risk and Risk Management:** The first possible risk is losing design data due to a server crash; therefore, multiple copies of the design will be saved on multiple servers. The second risk is device damage due to mishandling. To minimize the risk, we will wear ESD anti-static wristbands and minimize the time the integrated circuit is handled.

- **3.1.8 Project Proposed Milestones and evaluation Criteria:** The following step will represent general milestones of the project and the way they will be evaluated:
  - Research Delta Sigma ADC literature and understand the structure of the design. Evaluation: to get a general block diagram of the design.
  - Design Temperature Sensor. Evaluation: Simulation results.
  - Design Switched Capacitor Filter. Evaluation: Simulation results.
  - Design Operational Amplifier. Evaluation: Simulation results.
  - Design Switched Capacitor Integrator Filter. Evaluation: Simulation results.
  - Design Dynamic Comparator Evaluation: Simulation results.
  - Design 1-bit DAC Evaluation: Simulation results.
  - Design the ADC's Modulator. Evaluation: simulation results.
  - Design and test the Decimator unit. Evaluation: Simulation results.
  - Assemble all sub part and test for cumulative output results Evaluation: Simulation results.
  - Create layouts for each circuit and compile the layouts to form the data converter.
  - Test and run simulations after extracting parasitic capacitances.

Figure 3.1 shows the proposed design process flow. Sub-parts are designed individually and get tested in ideal configuration. After each sub-part is tested in an ideal situation, the part's physical layout is made. A non-ideal circuit that considers the parasitic capacitance of the transistors and interconnects is extracted from this layout and its performance is then compared with the performance of the ideal circuit to ensure that it behaves as desired.

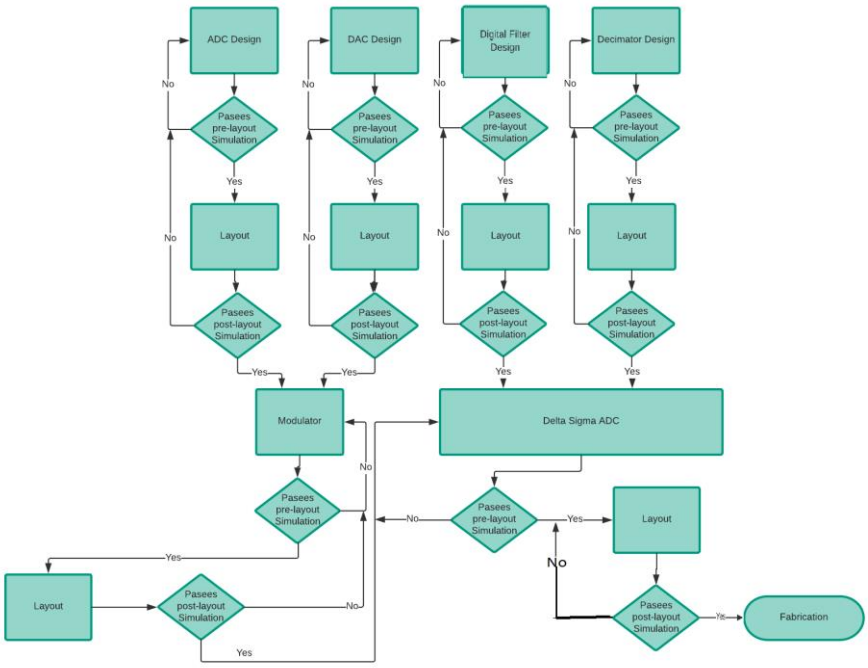

Figure 3.1: Design Process Flow Chart

Although there are many kinds of ADCs, delta-sigma ADCs dominate the digital world because unlike other architectures, they offer high resolution, high speed, accurate measurements, low power dissipation, and low cost. However, one of the biggest drawbacks is the large cycle latency from input to output, but this is not a problem since Delta-Sigma ADCs are used with a low-frequency input signal for this application.

Once again, an alternative design could be a successive approximation register (SAR) architecture. An advantage of using this type of architecture is that it allows for zero cycle latency. However, SAR ADCs do not provide the same level of sampling rate nor the output bits of resolution that the delta-sigma architecture does, so the delta-sigma architecture is best for our application[14].

3.2 Verification and Validation

- **3.2.1 Temperature Sensor:** The temperature sensor design uses a PTAT (proportional to absolute temperature) circuit architecture. This architecture uses diode connected transistors to translate the temperature to a temperature-dependent current, then converts this current to a temperature-dependent voltage at the output. The output voltage is fed to the input of the ADC.

  The desired output of the sensor is a voltage that has a linear relationship with the temperature of the circuit. To test the linearity of the sensor, we will run a DC (Direct Current) simulation in Cadence Virtuoso using the temperature sweep function to see if

the relationship between output voltage and temperature is as expected within the temperature range of operation.

- **3.2.2 Integrator:** It should take an analog voltage from the temperature sensor and one of two possible voltage outputs from the 1-bit DAC at the input. It should add these voltages using two switched-capacitor circuits, then use an op-amp integrator in feedback configuration to produce a saw-tooth waveform at the output whose slopes are proportional to the magnitude of the analog voltage input from the temperature sensor. The functionality will be tested using schematic simulation in Cadence Virtuoso. The inputs will be simulated using ideal voltage sources. The voltage source corresponding to the temperature sensor will be set at a value that corresponds to a point within the output range of the temperature sensor when the temperature is in the range of interest. The voltage source corresponding to the 1-bit DAC will be set to one of its possible output values. A transient simulation will be executed, and the time taken for the output voltage of the integrator to traverse its designated output range will be measured. The DAC will then be set to its other possible output value, and the measurement will be repeated. The ratio of the two measurements should be equal to the ratio of the distances between the output voltage of the temperature sensor and each of the ends of the temperature sensor's output range.
- **3.2.3 Comparator:** A sawtooth wave will be applied at the non-inverting input, and a DC voltage will be applied to the inverting input, this will be the reference voltage. A high-frequency clock signal will be applied to the comparator as well. The comparator should read the input waveform at each clock edge. When the voltage at the non-inverting input is less than the voltage at the inverting input the output signal will be low, when the voltage at the non-inverting input is greater than the voltage at the inverting input the output signal will be high. The sawtooth wave will allow us to see the output change from a low to high level as the input ramps up. This will allow us to confirm the operation of the comparator, such that it compares the voltages at the two inputs and produces either a high or low output.
- **3.2.4 1-Bit DAC:** It should take a 1-bit digital signal and output an analog value represented as a voltage. This will be tested using schematic simulation in Cadence Virtuoso. The input to the DAC will be a stepping binary signal that will step from 0 to 1. The DAC should then output either a $+V_{REF}$ or a $-V_{REF}$. This reference voltage will be determined by an additional biasing circuit that will also be used for the reference voltage for the comparator. If we draw a fit line between these two points, the line is forced to be linear due to only having two points to draw the line between. This allows the DAC to behave as an ideal DAC and eliminates the need for calibration.
- **3.2.5 Digital Decimator and Low-pass Filter:** It should take in a 1-bit digital signal from the comparator and output a 10-bit digital value. This will be tested using Modelsim, with a pass being considered as different input data streams (corresponding to different temperature readings) resulting in 10-bit output values representing the temperature

values being input from the comparator. There should be one output value for every 1024 clock cycles. In addition, this behavior should be the same when connected with the other components after conversion using Encounter RTL.

- **3.2.6 Complete Circuit:** Once all the components have been tested and proper functionality has been confirmed, they will be connected together in Cadence Virtuoso and the complete circuit will be tested using schematic simulation.

  The temperature of the circuit, which serves as the input of the system, will be controlled using an option in the SPECTRE simulator. This parameter will be swept across the range of values corresponding to the project's temperature range of interest, and the resulting binary digital output values will be recorded. These output values will then be compared to the input voltages at various points to verify proper functionality of the circuit. After proper functionality is verified, the parasitic capacitances will be extracted, and the simulation will be repeated with these capacitances considered. If the performance of the circuit is found to have been degraded, then these capacitances will be compensated for in the circuit and simulation will be repeated until proper functionality is verified.

  After the circuit has been fabricated and we have received the IC in its package, we will perform post-fabrication testing. The IC will be placed on a breadboard and put in an oven which will allow us to control its temperature. The circuit's output pins will be connected to a PC interface card which will allow us to view the output values from the circuit on a computer screen. We will set the oven to various temperatures within the project's temperature range of interest and record the resulting output values. We will repeat these measurements several times and compare the sets of measurements to each other to determine the circuit's precision. We will then average these sets of measurements and compare them with a plot of the expected output value vs. temperature plot to determine the circuit's accuracy.

4 Estimated Resources and Project Timeline

4.1 Personal Effort requirements

Individual Tasks: Temperature Sensor, Switched Capacitor Integrator, Comparator (1-bit ADC), 1-bit DAC, Digital Decimator

These tasks will be completed by:

- Each task should be researched thoroughly. Each team member will design a schematic for a different circuit component.
  - 7 hours per week should be dedicated by each member during the research and schematic design stage.
- The schematics should be built and simulated
  - 10 hours per week should be dedicated by each member during the schematic building and simulation stage
- Pre-layout simulations should be run
  - 15 hours per week should be dedicated during the pre-layout simulation stage

- The layout for the schematic should be created
    - 15 hours per week should be dedicated during the layout stage
- Post-layout simulations should be run
    - 20 hours per week should be dedicated during the post-layout simulation stage

Testing After Combining: Each subcomponent will be combined, and the full circuit will be tested.

This will be completed by:

- The complete delta-sigma modulator including the switched capacitor integrator, comparator, and 1-bit DAC should be tested and verified to function correctly as a complete subsystem. Correct functionality will be shown by the presence of an output data stream whose proportion of 1's to 0's in a 10-millisecond timespan is proportional to the magnitude of the input voltage relative to the input voltage range. 20 hours will be dedicated to testing this subsystem once it is completed.
- The digital decimator should be connected to the output of the delta-sigma modulator and verified to function correctly. Correct functionality will be shown by the presence of 10-bit parallel binary output codes, output at a rate of one every 10 milliseconds, whose magnitudes are proportional to the magnitude of the input voltage relative to the ADC input voltage range. 20 hours will be dedicated to testing the delta-sigma modulator and digital decimator connected after completion of both subsystems.
- The temperature sensor should be attached at the input of the ADC and should be tested and verified to function correctly. Correct functionality will be shown by the presence of 10-bit parallel binary output codes, output at a rate of one every 10 milliseconds, whose magnitudes are proportional to the magnitude of the chip's temperature relative to the 10-degree to 60-degree Celsius range. 20 hours will be dedicated to testing the delta-sigma modulator and digital decimator connected after completion of both subsystems.

Layout of Individual Tasks: Each person will do the layout for their respective components upon completion of schematic testing.

This will be completed by:

- Each task's layout will be individually designed using Cadence.
    - 15 hours a week will be dedicated to designing the individual task's layout.
- The layouts will be combined.
    - 10 hours a week will be dedicated to combining the layouts.
- Post-layout simulations will be done to ensure no issues exist within the layout.
    - 20 hours a week will be dedicated to performing post layout simulations.

Ensure for Fabrication: Last minute checks before sending the circuit to be fabricated.

This will be completed by:

- Ensuring that the circuit will function as intended to the best of our abilities.
    - 20 hours a week will be dedicated to ensuring that the circuit has no flaws before fabrication.

Testing After Fabrication: Verify circuit functionality once we receive the package from MOSIS.

This will be completed by:

- Performing numerous tests on the fabricated circuit.
- Troubleshooting the circuit to the best of our abilities.
    - 15 hours a week will be dedicated to testing and troubleshooting the fabricated circuit.

Documentation: Documents provided detail on our circuit.

This will be completed by:

- Documenting the project on a weekly basis throughout the next two semesters.
    - 10-15 hours a week will be dedicated to documenting the project.

4.2 Resources needed

The resources our team requires includes access to the following: Cadence, fabrication through MOSIS, IEEE libraries, TSMC 180nm process, 180nm files for Cadence. Our team will be fabricating the integrated circuit in Taiwan Semiconductor Manufacturing Company's 180nm process[15]. Using the 180nm process will limit us to a 1.8V voltage supply, transistor sizes with widths larger than 300 nm and lengths larger than 200 nm, and other parameters inherent to the 180nm process. The parameters include: μCox, V_{TO}, λ. These parameters will determine the design of our circuits. The bonding pad is being provided to us by the ECPE graduate students and will follow the 180nm process.

IEEE standards need to be implemented during fabrication and testing of the Delta Sigma data converter. The two standards mainly used are the IEEE Standard for Terminology and Test Methods for Analog to Digital Converter[16] and the IEEE Standard for Nano manufacturing -large scale manufacturing for nanoelectronics[17]. The IEEE Standard for Terminology and Test Methods for Analog to Digital Converter outlines testing methods that will allow us to characterize the data converter and determine the quality of its functionality. Following this standard will ensure that our testing results are accurate and that we use standard industry practices and reporting to allow the performance of our device to be easily compared to that of other ADCs. The IEEE Standard for Nano manufacturing -large scale manufacturing for nanoelectronics outlines standards and methods that will be followed by MOSIS when fabricating the data converter.

4.3 Financial Resources needed

As of now our team requires very little financial resources. The fabrication costs for a circuit the same size as ours is typically around $20,000. MOSIS will be fabricating our circuit and has a program with universities, where they offer fabrication biannually completely sponsored by them, thus Iowa State does not need to contribute any funds for the fabrication of the data converter. MOSIS only fabricates integrated circuit for academic purposes after each semester, so it is essential that by May 5, 2018 the circuit is ready for fabrication. If the circuit is not ready by the previously stated date, the project cannot continue. Our team will need to purchase a National Instruments serial interface card, this will be around $180. The serial interface card will be used to read the parallel digital output of the data converter and output it to a USB, allowing us to read it on a computer screen.

4.4 Project Schedule

	Week of:														
	2/5 - 2/11	2/12 - 2/18	2/19 - 2/25	2/26 - 3/4	3/5 - 3/11	3/12 -3/18	3/19 -3/25	3/26 - 4/1	4/2 - 4/8	4/9 - 4/15	4/16 - 4/22	4/23 - 4/29	4/30 - 5/4	8/20 -12/3	12/3- 12-14
Stage															
Individual Tasks	5 weeks														
Combining Tasks and Testing						4 weeks									
Layout of Individual Tasks										2 weeks					
Ensure For Fabrication												2 weeks			
Testing Post-Fabrication														12 weeks	
Finishing Documentation															2 weeks

Figure 4.1: Project Timeline

5 Closure Materials

5.1 Closing Summary

To properly design a Delta-Sigma ADC, there are many design and implementation challenges that will be faced. The design must fit the needs of the eventual use case of Drs. Geiger and Chen and be able to implement itself properly in their larger research needs. They need a high resolution, low latency ADC for temperature measurement in the circuits they are building. Our design approach means adhering to a strict and rigid set of design requirements and considering their needs in the design process. The basic structure of the design will include the delta-sigma modulator, digital filter, and decimator. The modulator will be designed with a difference amplifier, integrator, ADC, and DAC to output to the digital filter. These steps ensure that the design retains a high-resolution element, while being relatively simplistic so to keep budget and time constraints low. This makes it feasible to complete the design phase of the project within the first semester, leaving the second semester for thorough testing after fabrication.

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